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E Rotenberg
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ISDL: An **Instruction** Set Description Language For Retargetability - all 11 versions »
G Hadjiyiannis, S Hanono, S Devadas - Design Automation Conference, 1997. Proceedings of the 34th, 1997 - ieeexplore.ieee.org
... as input to the **Instruction** Level **Simulator** (ILS ... ProgramCounter(**width**) Wire(**width**) - Interconnect for datapath ... D. **Instruction** Set The **Instruction** Set section is ...
Cited by 200 - Related Articles - Web Search

Dynamically Exploiting Narrow **Width** Operands to Improve Processor Power and Performance - all 18 versions »
D Brooks, M Martonosi - Proceedings of the The Fifth International Symposium on High ..., 1999 - doi.ieeecomputersociety.org
... (Section 3 will discuss the Alpha compiler and SimpleScalar **simulator** used to ... We will refer to these operands as narrow-**width**; an **instruction** execution in ...
Cited by 152 - Related Articles - Web Search

[PDF] An accurate and fine grain **instruction**-level energy model supporting software optimizations - all 3 versions »
S Steinke, M Knauer, L Wehmeyer, P Marwedel - Proc. of PATMOS - patmos2001.eivd.ch
... Furthermore, the **simulation** results of these models are not ... The **instruction**-dependent costs in the **instruction** memory (Word **width** = **bit width** of memory ...
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Path-Based Next Trace Prediction - all 26 versions »
Q Jacobson, E Rotenberg, JE Smith - Proceedings of the 30th International Symposium on ..., 1997 - doi.ieeecomputersociety.org
... **Width bits** ... To study predictor performance, trace driven **simulation** with the Simplescalar tool set is used [1]. Simplescalar uses an **instruction** set largely ...
Cited by 132 - Related Articles - Web Search

Analytical energy dissipation models for low power caches - all 8 versions »
MB Kamble, K Ghosse - Low Power Electronics and Design, 1997. Proceedings., 1997 ..., 1997 - ieeexplore.ieee.org
... **width**, line **width**, cache capacity etc. ... CAPE is a detailed register level CPU **simulator** ... B proceeds as follows: 1))W :Allofthe tag, data and status **bits** in the ...
Cited by 286 - Related Articles - Web Search

[BOOK] Trace Cache: A Low Latency Approach to High Bandwidth **Instruction** Fetching - all 65 versions »
E Rotenberg, S Bennett, J Smith - 1996 - University of Wisconsin-Madison, Computer Sciences Dept
... **Simulation** results are presented in Section 5. As part of ... constraint is imposed by the **width** of the ... The leading zeroes in the valid **instruction bit** vectors are ...
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A Large, Fast **Instruction** Window for Tolerating Cache Misses - all 16 versions »
AR Lebeck, J Koppanalil, T Li, J Patwardhan, E ... - ieeexplore.ieee.org
... We also modified the **simulator** to warm up the ... across the banks, interleaving at the individual **instruction** granularity ... 2K entry WIB with a dispatch **width** to the ...
Cited by 112 - Related Articles - Web Search

Thumb: Reducing the Cost of 32-bit RISC Performance in Portable and Consumer applications - all 7 versions »
L Goudge, S Segars - Proceedings of COMPCON, 1996 - doi.ieeecs.org
... can either debug code running on an **instruction** accurate **simulator** ... The **simulator** can be configured to emulate target hardware ... Mode Bus **width** 5 MHz 10MHz 40 MHz ...
Cited by 24 - Related Articles - Web Search

The SimpleScalar tool set, version 2.0 - all 104 versions »
D Burger, TM Austin - ACM SIGARCH Computer Architecture News, 1997 - portal.acm.org
... icompress remap SimpleScalar's 64--**bit instructions** to a 32-**bit** equivalent in the **simulation** (ie, model a machine with 4-word **instructions**). ...
Cited by 1148 - Related Articles - Web Search

A system-level energy minimization approach using datapath **width** optimization - all 20 versions »
Y Cao, H Yasuura - Proceedings of the 2001 international symposium on Low power ..., 2001 - portal.acm.org
... Dynamic analysis is one kind of **simulation**-based method ... data is executed by only

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S Bennett
E Rotenberg
S Palacharla
D Burger

ISDL: An **Instruction** Set Description Language For Retargetability - all 11 versions »
G Hadjiyiannis, S Hanono, S Devadas - Design Automation Conference, 1997. Proceedings of the 34th, 1997 - ieeexplore.ieee.org
... as input to the **Instruction** Level **Simulator** (ILS ... ProgramCounter(**width**) Wire(**width**) - Interconnect for datapath ... D. **Instruction** Set The **Instruction** Set section is ...
Cited by 200 - Related Articles - Web Search

[BOOK] Trace Cache: A Low Latency Approach to High Bandwidth **Instruction** Fetching - all 65 versions »
E Rotenberg, S Bennett, J Smith - 1996 - University of Wisconsin-Madison, Computer Sciences Dept
... **Simulation** results are presented in Section 5. As part of ... constraint is imposed by the **width** of the ... The leading zeroes in the **valid instruction bit** vectors are ...
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Increasing the **instruction** fetch rate via multiple branch prediction and a branch address cache - all 6 versions »
TY Yeh, DT Marr, YN Patt - Proceedings of the 7th international conference on .... 1993 - portal.acm.org
... an **instruction** cache with enough band- **width** to supply ... Section 3.3 discusses the **instruction** cache design is- ... used, and Section 5 shows our **simulation** results. ...
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Analytical energy dissipation models for low power caches - all 8 versions »
MB Kamble, K Ghosse - Low Power Electronics and Design, 1997. Proceedings., 1997 .... 1997 - ieeexplore.ieee.org
... **width**, line **width**, cache capacity etc. ... CAPE is a detailed register level CPU **simulator** ... B proceeds as follows: 1))W :Allofthe tag, data and status **bits** in the ...
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MIPS-X: a 20-MIPS peak, 32-bit microprocessor with on-chip cache - all 3 versions »
M Horowitz, P Chow, D Stark, RT Simoni, A Salz, S ... - Solid-State Circuits, IEEE Journal of, 1987 - ieeexplore.ieee.org
... **width** requirements, MIPS-X includes a 2-kbyte on-chip **instruction** cache ... All 37 **instructions** are 32 **bits** and use a fixed format ... The result of the **instruction** is ...
Cited by 61 - Related Articles - Web Search

Instruction Set Compiled **Simulation**: A Technique for Fast and Flexible **Instruction** Set **Simulation** - all 17 versions »
M Reshadi, P Mishra, N Dutt - Design Automation Conference (DAC), 2003 - doi.ieeecomputersociety.org
... For instance, the ARM processor uses the Thumb (reduced **bit-width**) **instruction** set to reduce power and ... Thus, our **instruction** set compiled **simulation** (IS-CS ...
Cited by 48 - Related Articles - Web Search

Exploiting data-**width** locality to increase superscalar execution bandwidth - all 8 versions »
GH Loh - Microarchitecture, 2002.(MICRO-35). Proceedings. 35th Annual ..., 2002 - ieeexplore.ieee.org
... number of **instructions** skipped before the start of **simulation**. ... For every dynamic icomp **instruction**, we classify it as short-sized if its data- **width** is 16 ...
Cited by 27 - Related Articles - Web Search

Saving energy with just in time **instruction** delivery - all 7 versions »
T Karkhanis, JE Smith, P Bose - Proceedings of the 2002 international symposium on Low power ..., 2002 - portal.acm.org
... mented at granularity equal to the pipeline **width**. ... switching network connecting all the **instruction** slots within and ... Our **simulation** model also differs in other ...
Cited by 21 - Related Articles - Web Search

Runahead execution: an alternative to very large **instruction** windows for out-of-order processors - all 22 versions »
O Mutlu, J Stark, C Wilkerson, YN Patt - High-Performance Computer Architecture, 2003. HPCA-9 2003. ..., 2003 - ieeexplore.ieee.org
... The **simulator** includes a detailed memory subsystem that fully models buses and bus con- tention. ... Fetch/Issue/Retire **Width** 3 6 ... **Instruction** window size 128 512 ...
Cited by 111 - Related Articles - Web Search

System for simulating memory arrays in a logic **simulation** machine - all 2 versions »
AM Rudy - US Patent 4,862,347, 1989 - Google Patents
... All array **instructions** representing the same memory array share the same address space in the real ... **SIMULATION** PR OFI LE MEMORY ... READ DATA **BITS** 0-15 FOR INSTR I ...
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All Results

S Goldstein
R Rosin
G Frieder
A DeHon
H Schmit

Did you mean: ***simulation*** + instruction + width + bits

A time-multiplexed FPGA architecture for logic **emulation** - all 3 versions »
D Jones, DM Lewis - Custom Integrated Circuits Conference, 1995., Proceedings of ..., 1995 - ieeexplore.ieee.org
... interconnect is used in a Xilinx -based **emulator** at some ... SI S = SL+UxS,+J. The smallest average **instruction** size is 84.4 **bits**, occurring at a **width** of 16 ...
Cited by 43 - Related Articles - Web Search - Library Search

RISC architecture computer configured for **emulation** of the **instruction** set of a target computer - all 3 versions »
HL Scantlin - US Patent 5,574,927, 1996 - Google Patents
... the RHS to configure the **emulation** register 40 ... the size required for the par -ticular emulated **instruction**. Similarly, this field determines the **width** of the ...
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PipeRench: a reconfigurable architecture and compiler - all 7 versions »
SC Goldstein, H Schmit, M Budiu, S Cadambi, M Moe, ... - Computer, 2000 - ieeexplore.ieee.org
... in a single static configuration rather than an instruc- tion sequence, reducing **instruction** band- **width** and control overhead. ... operate on **bit** widths that ...
Cited by 216 - Related Articles - Web Search

... internal sixteen bit operation or internal eight bit operation in accordance with an **emulation** bit - all 2 versions »
WD Mensch Jr - US Patent 4,876,639, 1989 - Google Patents
... If the **emulation bit** is set to a "0", the 16 ... an **instruction** set of which the 6502 **instruction** set is ... iMEMORY 8 REGISTER **WIDTH** DECODE 1ST TRANSFER SIGNALS **BITS** ...
Cited by 24 - Related Articles - Web Search

The density advantage of configurable computing - all 7 versions »
A DeHon - Computer, 2000 - ieeexplore.ieee.org
... **Emulation**. ... With less **instruction** overhead, the ... result, processors often waste a portion of their computational capacity when operating on narrow-**width** data ...
Cited by 199 - Related Articles - Web Search

Extended floating point operations supporting **emulation** of source **instruction** execution - all 3 versions »
JA Mitchell, JF Bechdel - US Patent 4,841,476, 1989 - Google Patents
... sequence which reduces the number of cycles re- 10 a corresponding **width** for the data and **instruction** ... When used as an **emulator**, the target CPU operates ...
Cited by 59 - Related Articles - Web Search

... for inserting a bus cycle in an **instruction** set to output an internal information for an **emulation** - all 3 versions »
S Matsui, I Kawasaki, Y Kondo, K Hashimoto - US Patent 5,564,041, 1996 - Google Patents
... In an **emulation** of the system using the **instruction** prefetch type ... «„„ **INSTRUCTION** CODE PO INTER PRO COU CRAM -_ ... UNIT p*"] »P MICRO son isy L ti **Bit**- Ms ...
Cited by 21 - Related Articles - Web Search

Scalable **width** vector processor architecture for efficient **emulation** - all 3 versions »
SP Song, H Park... - US Patent 5,991,531, 1999 - Google Patents
... Most instmctions are independent of data **width** and are ... Vector processor **instructions** may specify a location ... can be defined or modified for 64-byte **emulation**. ...
Cited by 9 - Related Articles - Web Search

An environment for research in microprogramming and **emulation**
RF Rosin, G Frieder, RH Eckhouse Jr - Communications of the ACM, 1972 - portal.acm.org
... The 16-**bit width** of this store was selected to ... the **instructions** and constants of an **emulator**, with data ... The basic **instruction** format of these words is usually ...
Cited by 51 - Related Articles - Web Search - Library Search

[PDF] Wabi CPU **emulation** - all 3 versions »
P Hohensee, M Myszewski, D Reese - Proceedings Hot Chips VIII, 1996 - hotchips.org
... q Shortage of host registers for x86 and **emulator** state ... 50% of x86 **instructions** reference memory – 90% of memory references are non-byte **width** ...

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All Results

E Marinissen
Y Zorian
R Kapur
L Whetsel
D Patterson

Towards a Standard for Embedded Core **Test**: An Example - all 8 versions »
EJ Marinissen, Y Zorian, R Kapur, T Taylor, L ... - Proceedings IEEE International **Test** Conference (ITC), 1999 - doi.ieeecomputersociety.org
... If no new **instructions** are loaded, the serial **interface** si/so doubles as **interface** to the ... principal function of the parallel TAM is to **test** the core ...
Cited by 130 - Related Articles - Web Search

On Using IEEE P1500 SECT for **Test** Plug-n-Play - all 8 versions »
EJ Marinissen, R Kapur, Y Zorian - Proceedings IEEE International **Test** Conference (ITC), 2000 - doi.ieeecomputersociety.org
... design, in the way that its **interface**, consisting of ... loading **instructions** into the Wrapper **Instruction** Register, as well as for low-bandwidth **test** data access ...
Cited by 61 - Related Articles - Web Search

A new network processor architecture for high-speed communications - all 3 versions »
X Nie, L Gazsi, F Engel, G Fettweis - Signal Processing Systems, 1999. SiPS 99. 1999 IEEE Workshop ..., 1999 - ieeexplore.ieee.org
... separated for the communication **interface** data from ... The SUBI **instruction** decrements the counter and a ... For IF-statements **test instructions** operating on variable ...
Cited by 54 - Related Articles - Web Search

An approach to **interface** synthesis - all 11 versions »
J Madsen, B Hald - Proceedings of the 8th international symposium on System ..., 1995 - portal.acm.org
... b) . (? i **TEST** k ! d : d = 1) + . (i RES k ... Notice the introduction of **instruction** invocations in the ... channel is thus the outcome of **interface** synthesis ...
Cited by 47 - Related Articles - Web Search

Design and **Test** of Large Embedded Memories: An Overview - all 5 versions »
R Rajsuman - ieeexplore.ieee.org
... s An on-chip memory **interface** replaces large off-chip drivers with small on-chip drivers. ... 18 IEEE Design & **Test** of Computers ... GDSII Spice netlist **Width** (**bits**) ...
Cited by 37 - Related Articles - Web Search

Selective **instruction** compression for memory energy reduction in embedded systems - all 5 versions »
L Benini, A Macii, E Macii, M Poncino - Proceedings of the 1999 international symposium on Low power ..., 1999 - portal.acm.org
... Bus encoding schemes reduce **interface** power by changing the ... the **bit-width** of the compressed **instructions** (ie, 8 ... the size of the **instruction** decompression table ...
Cited by 79 - Related Articles - Web Search

A case for intelligent RAM - all 15 versions »
D Patterson, T Anderson, N Cardwell, R Fromm, K ... - Micro, IEEE, 1997 - ieeexplore.ieee.org
... a processor could sig- nificantly increase the **test** time on ... Next, since misses from the **instruction** and data caches ... we can have a much wider **interface** on chip ...
Cited by 257 - Related Articles - Web Search

A methodology for the design of application specific instructionset processors (ASIP) using the ... - all 11 versions »
A Hoffmann, O Schliebusch, A Nohl, G Braun, O ... - Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM ..., 2001 - ieeexplore.ieee.org
... cost and performance for the configuration wider **test**. ... well defined ap- plication programming **interface** (API) to interconnect the **instruction**-set simulator ...
Cited by 21 - Related Articles - Web Search

Reduced **instruction** set computer system including apparatus and method for coupling a high ... - all 3 versions »
WM Johnson, TA Olson, DJ Dutton, S Lee, DW Stoenner ... - US Patent 5,317,715, 1994 - Google Patents
... INTR •**TEST** MSERR *RESET ... According to the invention, a reduced **instruction** set ... The novel system **interface** taught in the 40 methods for coupling a high ...
Cited by 25 - Related Articles - Web Search

On IEEE P1500's Standard for Embedded Core **Test** - all 4 versions »
EJ Marinissen, R Kapur, M Lousberg, T McLaurin, M ... - Journal of Electronic Testing, 2002 - Springer
... This captured data may be used for **test** control, testing of the WIR ... Wrapper **Interface** Port ... connected between WSI and WSO for loading an **instruction**, or whether ...

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All Results
E Marinissen
R Kapur
Y Zorian
J Edmondson
M Lousberg

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EJ Marinissen, Y Zorian, R Kapur, T Taylor, L ... - Proceedings IEEE International **Test** Conference (ITC), 1999 - doi.ieeecomputersociety.org
... If no new **instructions** are loaded, the serial **interface** si/so doubles as **interface** to the ... principal function of the parallel TAM is to **test** the core ...
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UltraSPARC: the next generation superscalar 64-bit SPARC - all 6 versions »
D Greenley, J Bauman, D Chang, D Chen, R Eltejaein ... - Compcon'95.'Technologies for the Information Superhighway', ..., 1995 - ieeexplore.ieee.org
... Unit 4 __ System External **Interface** Cache RAM ... PDU) includes a high band- **width** **instruction** prefetch engine that ... **instructions** in a 12-deep **instruction** buffet To ...
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On Using IEEE P1500 SECT for **Test** Plug-n-Play - all 8 versions »
EJ Marinissen, R Kapur, Y Zorian - Proceedings IEEE International **Test** Conference (ITC), 2000 - doi.ieeecomputersociety.org
... design, in the way that its **interface**, consisting of ... loading **instructions** into the Wrapper **Instruction** Register, as well as for low-bandwidth **test** data access ...
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Pipelined processor with two tier prefetch buffer structure and method with bypass - all 2 versions »
RJ Divivier, M Nemirovsky - US Patent 5,680,564, 1997 - Google Patents
... prefetch buffers, prefetch buffer 0, is the **interface** between pipeline. ... ticular combination of the **valid bits** of the two prefetch ... able **width** **instruction** sets. ...
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A 9-ns HIT-delay 32-kbyte cache macro for high-speed RISC - all 4 versions »
K Nogami, T Sakurai, K Sawada, K Sakaue, Y ... - Solid-State Circuits, IEEE Journal of, 1990 - ieeexplore.ieee.org
... Perfor- mance of the **test** device is summarized in Section ... which is about 50 MHz in I'IL **interface**. ... With the double-word load/store **instruction**, the RISC can ...
Cited by 34 - Related Articles - Web Search

[PDF] Internal Organization of the Alpha 21164, a 300-MHz 64-bit Quad-issue CMOS RISC Microprocessor - all 6 versions »
JH Edmondson, PI Rubinfeld, PJ Bannon, BJ ... - Digital Technical Journal, 1995 - python.planetmirror.com
... CACHE CONTROL AND BUS **INTERFACE** UNiT ... a conditional move or a branch **test** input operand ... issue **width** increases, the cost in **instruction** execution opportunities ...
Cited by 133 - Related Articles - View as HTML - Web Search

MIPS-X: a 20-MIPS peak, 32-bit microprocessor with on-chip cache - all 3 versions »
M Horowitz, P Chow, D Stark, RT Simoni, A Salz, S ... - Solid-State Circuits, IEEE Journal of, 1987 - ieeexplore.ieee.org
... **width** requirements, MIPS-X includes a 2-kbyte on-chip ... 1 **Instructlon** Regrster ... bypass registers, and the registers associated with the external memory **interface**. ...
Cited by 61 - Related Articles - Web Search

Motorola MC 68020. - all 4 versions »
D MacGregor, D Mothersole, B Moyer - IEEE Micro, 1984 - ieeexplore.ieee.org
... for modular programming, and provides a coprocessor **interface** for **instruction** ... units, and an on-board **instruction** cache. ... the 32-**bit** data bus **width**, the presence ...
Cited by 8 - Related Articles - Web Search

[PDF] On-line Testing of an Off-the-shelf Microprocessor Board for Safety-critical Applications - all 5 versions »
F Corno, M Damiani, L Impagliazzo, P Prinetto, M ... - EDCC Conference, Taormina (Italy), 1996 - elite.polito.it
... the dynamic data from one part to the other, and then forcing the processor to fetch **instructions** from the ... Third, the **test** of the **interface** devices between ...
Cited by 7 - Related Articles - View as HTML - Web Search

A methodology for the design of application specific instructionset processors (ASIP) using the ... - all 11 versions »
A Hoffmann, O Schliebusch, A Nohl, G Braun, O ... - Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM ..., 2001 - ieeexplore.ieee.org
... cost and performance for the configuration wider **test**. ... well defined ap- plication programming **interface** (API) to interconnect the **instruction**-set simulator ...
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D Lentz
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S Garg

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RISC architecture computer configured for **emulation** of the **instruction** set of a target computer - all 3 versions »
HL Scantlin - US Patent 5,574,927, 1996 - Google Patents
... the RHS to configure the **emulation** register 40 ... the size required for the par -ticular emulated **instruction**. Similarly, this field determines the **width** of the ...
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... internal sixteen bit operation or internal eight bit operation in accordance with an **emulation** bit - all 2 versions »
WD Mensch Jr - US Patent 4,876,639, 1989 - Google Patents
... If the **emulation bit** is set to a "0", the 16 ... an **instruction** set of which the 6502 **instruction** set is ... iMEMORY 8 REGISTER **WIDTH** DECODE 1ST TRANSFER SIGNALS **BITS** ...
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Dynamic memory disambiguation using the memory conflict buffer - all 5 versions »
DM Gallagher, WY Chen, SA Mahlke, JC Gyllenhaal, ... - Proceedings of the sixth international conference on ..., 1994 - portal.acm.org
... conflict; when the correspond- ing check **instruction** is encountered ... nature contains **bits** which contain a hashed version ... The access **width** field contains two **bits** ...
Cited by 99 - Related Articles - Web Search

Instruction decoder including **emulation** using indirect specifiers - all 4 versions »
JG Favor... - US Patent 5,794,063, 1998 - Google Patents
... f Fedecode **bits** for all ... An including **emulation** using indirect specifiers in accordance ... 5.794.063 56 **Instruction** decoder 220 has interface connections to the ...
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UltraSPARC: the next generation superscalar 64-bit SPARC - all 6 versions »
D Greenley, J Bauman, D Chang, D Chen, R Eltejaein ... - Compcon'95.'Technologies for the Information Superhighway', ..., 1995 - ieeexplore.ieee.org
... PDU) includes a high band- **width instruction** prefetch engine ... expands the **instructions** to 76 **bits**, and stores ... **instructions** in a 12-deep **instruction** buffet To ...
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Accelerated **instruction** mapping external to source and target **instruction** streams for near realtime ... - all 4 versions »
DE Fisk, RL Griffith, ME Homan, G Radin, WJ ... - US Patent 4,587,612, 1986 - Google Patents
... the fact that the target **instruction** had a **width** different than ... 4, there is shown the **emulator** 60 more target CPU multifield **instructions**; comprising the ...
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Motorola MC 68020. - all 4 versions »
D MacGregor, D Mothersole, B Moyer - IEEE Micro, 1984 - ieeexplore.ieee.org
... by a combination of the higher clock frequency at which the MC68020 operates, the 32-**bit** data bus **width**, the presence ofthe on-chip **instruction** cache, and the ...
Cited by 8 - Related Articles - Web Search

An environment for research in microprogramming and **emulation**
RF Rosin, G Frieder, RH Eckhouse Jr - Communications of the ACM, 1972 - portal.acm.org
... The 16-**bit width** of this store was selected to ... the **instructions** and constants of an **emulator**, with data ... The basic **instruction** format of these words is usually ...
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Emulator Architecture - all 4 versions »
EG Mallach - detail, 1975 - doi.ieeecomputersociety.org
... These gaps may exist in the execution of I/O **instructions**, the execution of infrequently used non-I/O **instructions**, and **emulator** control (including control ...
Cited by 6 - Related Articles - Web Search

Instruction decoder including two-way **emulation** code branching - all 4 versions »
JG Favor... - US Patent 5,920,713, 1999 - Google Patents
... that predecode **bits** for all eight **instruction** bytes are calcu ... 230 for decoding most macroinstructions, an **instruction** decoder **emulation** circuit 231 ...
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